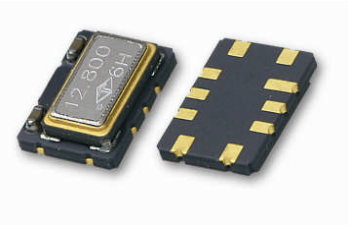
TS SERIES STRATUM III



The TS Stratum III series of oscillators feature an industry standard 7x5mm ceramic package designed for applications where space is at a premium and Stratum III frequency stability is required. This model is capable of +/-4.6ppm @ -40C ~ +85C, has very low power consumption, available CMOS and Clipped Sine Wave (without DC-cut capacitor) output, and VCTCXO pulling capability is optional. Popular uses of the TS Stratum III series include Telecommunication, Networking, and Satellite Communication.

Features:

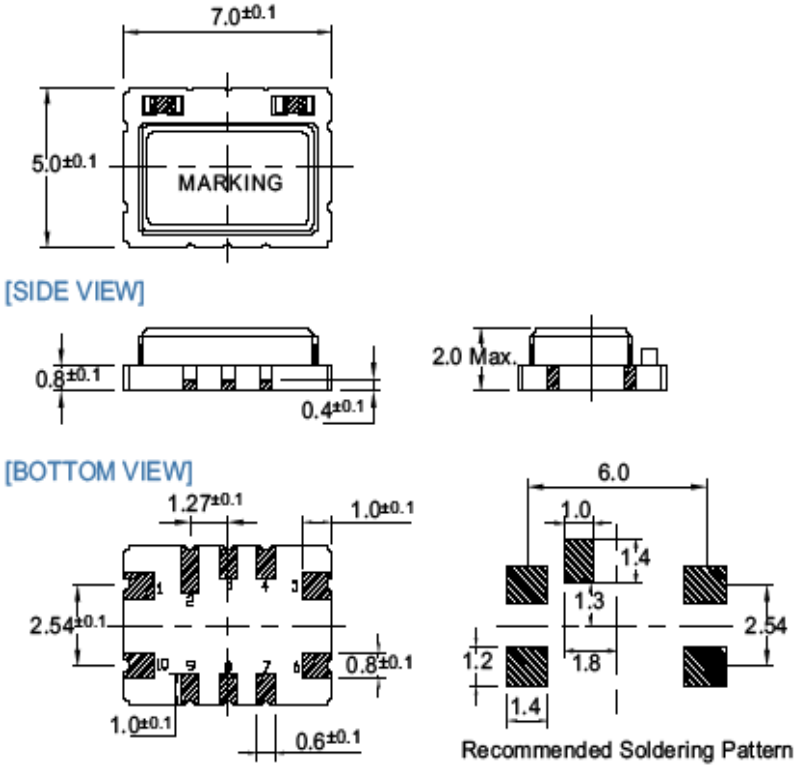
- Typical 7.0 x 5.0 x 2.0 mm ceramic SMD package
- Stratum 3 (Overall ±4.6 ppm including 20 years aging)
- CMOS and Clipped Sine wave (without DC-cut capacitor) output optional
- Packing: Tape & Reel 1000/3000 pcs per reel

Ordering Information

TCXO	Package (mm)	Supply Voltage (V)	Pulling Range (ppm)	Freq. Stability (ppm)	Temp. Range (°C)	Output Logic and Symmetry		Oscillator Mode	Appearance	Lead Free	Freq. (MHz)
TS Series Stratum III	L: 7.0 W: 5.0 H: 2.0	5 3.3	±5 ±8 TCXO	±4.6 (Including 20 Years Aging)	-20~+70 -40~+85	Output CMOS 15pF Clipped Sine Wave	Symmetry 50±5%	AT Fundamental * Not selectable by customer	Normal	RoHS Compliant	XX.XXXXXX

Ordering Example: TS stratum III series; VDD:3.3v; Pulling Range: ±5ppm; Freq. Stability∀4.6 (Including 20 Years Aging); Temp. Range: -40°C to +85°C; Load: CMOS 15pF, symmetry: 50±5%; AT Fundamental; Normal Appearance; RoH Compliant; Freq.: 12.800000 MHz.

Outline Drawing



PIN CONNECTIONS	
PIN	FUNCTION
1	VCON: VC-TCXO NC: TCXO
2	NC
3	NC
4	NC
5	GND
6	CMOS/CLIPPED SINE WAVE OUTPUT
7	NC
8	NC
9	TRI-STATE CONTROL*
10	VDD

*TRI-STATE:
1. Pad 9 > 70% VDD or NC: Output Enable
2. Pad 9 < 30% VDD or NC: Output Enable

Electrical Specification

Parameter	Min		Max.		Unit
	5.0	3.3	5.0	3.3	V
Supply Voltage Variation (V_{DD}) 5%	4.75	3.13	5.25	3.47	V
Frequency Range	10		26		MHz
Standard Frequency (for CMOS)	12.800				
Standard Frequency (for clipped sine)	10.00, 12.80, 19.20, 19.44, 25.60				
Operating Temperature Range	Refer to Ordering Information				ºC
Frequency Stability (Overall)	± 4.6				ppm
Frequency stability					
Vs Temperature Range (@-20ºC~+70ºC)	-		±0.28		ppm
Vs Temperature Range (@-40ºC~+85ºC)	-		±0.37		
Supply Current (CMOS output)	-		6		mA
Supply Current (Clipped Sine-wave output)	-		3.5		
Output Level (CMOS)					
Output High (Logic "1")	90% V_{DD}		-		V
Output Low (Logic "O")	-		10% V_{DD}		
Duty	45%		55%		%
Output Level (Clipped Sine Wave)	0.8		-		Vp-p
Vc Input Impedance	100		-		KΩ
Phase Noise @12.8 MHz					dBc/Hz
100 Hz	-120				
1 KHz	-140				
10 KHz	-148				
Start Time	-		2		mSec
Tri-state					V
Disable	-		(V_{DD})*20%		
Enable	(V_{DD})*80%		-		
Storage Temperature Range	-55		125		ºC